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# DAC7528

# CMOS Dual 8-Bit Buffered Multiplying
# DIGITAL-TO-ANALOG CONVERTER

## FEATURES

● **DOUBLE BUFFERED DATA LATCHES**

● **SINGLE 5V SUPPLY OPERATION**

● **±1/2 LSB LINEARITY**

● **FOUR-QUADRANT MULTIPLICATION**

● **DACs MATCHED TO 1%**

## APPLICATIONS

● **DIGITALLY CONTROLLED FILTERS**

● **DISK DRIVES**

● **AUTO CALIBRATION**

● **MOTOR CONTROL SYSTEMS**

● **PROGRAMMABLE GAIN/ATTENUATION**

● **X-Y GRAPHICS**

## DESCRIPTION

The DAC7528 contains two, 8-bit multiplying digital-to-analog converters (DACs). Separate on-chip latches hold the input data for each DAC to allow easy interface to microprocessors.

Each DAC operates independently with separate reference input pins and internal feedback resistors. Excellent converter-to-converter matching is maintained.

The DAC7528 operates from a single +5V power supply. The inputs are TTL-compatible. Package options include 20-pin plastic DIP and SOIC.
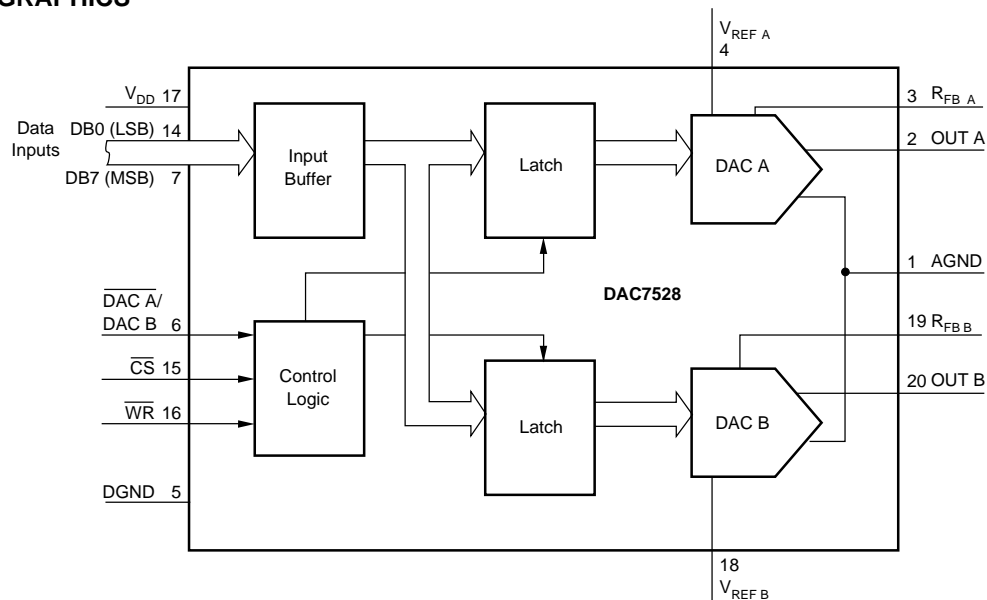
# SPECIFICATIONS

## ELECTRICAL

At $V_{DD}$ = +5V; $V_{REFA, B}$ = + 10V; $I_{OUT}$ = GND = 0V: T = Full Temperature Range specification under Absolute Maximum Ratings unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | DAC7528P, U | | | DAC7528PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **DC ACCURACY** [1] | | | | | | | | | |
| Resolution | N | | 8 | | | 8 | | | Bits |
| Relative Accuracy | INL | | | | ±1 | | | ±1/2 | LSB |
| Differential Nonlinearity | DNL | Guaranteed Monolithic Over Temp | | | ±1 | | | ±1/2 | LSB |
| FS Gain Error [2] | | $T_A$ = +25°C | | | ±2 | | | ±1 | LSB |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | ±4 | | | ±2 | LSB |
| Gain Tempco [2][3] | | | | ±2 | ±35 | | – | – | ppm/°C |
| Supply Rejection | PSR | $\Delta V_{DD}$ = ±5%, $T_A$ = +25°C | | 0.001 | 0.01 | | – | – | %FSR/% |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | 0.001 | 0.01 | | – | – | %FSR/% |
| Output Leakage Current (OUTA) | | DACA = $00_{16}$, $T_A$ = +25°C | | | ±50 | | | – | nA |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | ±200 | | | – | nA |
| Output Leakage Current (OUTB) | | DACB = $00_{16}$, $T_A$ = +25°C | | | ±50 | | | – | nA |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | ±200 | | | – | nA |
| **REFERENCE INPUT** | | | | | | | | | |
| Input Resistance | | ($V_{REFA}$, $V_{REFB}$) | 8 | 10 | 15 | – | – | – | kΩ |
| Input Resistance Match | | ($V_{REFA}$, $V_{REFB}$) | | | ±1 | | | – | % |
| **DYNAMIC PERFORMANCE** [4] | | | | | | | | | |
| Output Current Settling Time to 1/2 LSB | | Enable Pins Low $T_A$ = +25°C | | | 180 | | | – | ns |
| | | Load = 100Ω/13pF, $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 200 | | | – | ns |
| Digital-to-Analog Propagation Delay | | Enable Pins Low $T_A$= +25°C | | | 80 | | | – | ns |
| to 90% of Output | | Load = 100Ω/13pF, $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 100 | | | – | ns |
| Digital-to-Analog Impulse | | | | 125 | | | – | | nVs |
| AC Feedthrough | | $V_{REFA}$ = 20Vpp Sinewave, $T_A$ = +25°C | | | –70 | | | | dB |
| ($V_{REFA}$ to OUTA) | | 100kHz,$V_{REFB}$ = 0V, $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | –65 | | | | dB |
| AC Feedthrough | | $V_{REFA}$ = 20Vpp Sinewave, $T_A$ = +25°C | | | –70 | | | | dB |
| ($V_{REFB}$ to OUTB) | | 100kHz, $V_{REFB}$ = 0V, $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | –65 | | | | dB |
| Channel-to-Channel Isolation | | $V_{REFA}$ = 20Vpp Sinewave, 100kHz, | | –90 | | | – | | dB |
| ($V_{REFA}$ to OUTB) | | $V_{REFB}$ = 0V, Both DACs = $FF_{16}$ | | | | | | | |
| Channel-to-Channel Isolation | | $V_{REFB}$ = 20Vpp Sinewave 100kHz, | | –90 | | | – | | dB |
| ($V_{REFB}$ to OUTA) | | $V_{REFA}$ = 0V, Both DACs = $FF_{16}$ | | | | | | | |
| Digital Crosstalk | | Measured With Code Transition $00_{16}$ to $FF_{16}$ | | 30 | | | – | | nVs |
| Harmonic Distortion | THD | $V_{IN}$ = 6Vrms at 1kHz | | –85 | | | – | | dB |
| **ANALOG OUTPUTS** [4] | | | | | | | | | |
| OUTA capacitance | $C_{OUTA}$ | DAC = $00_{16}$ | | | 50 | | | – | pF |
| | | DAC = $FF_{16}$ | | | 120 | | | – | pF |
| OUTB capacitance | $C_{OUTB}$ | DAC = $00_{16}$ | | | 50 | | | – | pF |
| | | DAC = $FF_{16}$ | | | 120 | | | – | pF |
| **DIGITAL INPUTS** | | | | | | | | | |
| Input High Voltage | $V_{IH}$ | | 2.4 | | | – | | | V |
| Input Low Voltage | $V_{IL}$ | | | | 0.8 | | | – | V |
| Input Current | $I_{IN}$ | $T_A$ = +25°C | | | ±1 | | | – | µA |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | ±10 | | | – | µA |
| Input Capacitance [4] | $C_{IN}$ | All Digital Inputs | | | 10 | | | – | pF |
| **POWER REQUIREMENTS** | | | | | | | | | |
| Supply Current | $I_{DD}$ | Digital Inputs = $V_{IH}$ or $V_{IL}$, $T_A$ = +25°C | | | 1 | | | – | mA |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 1 | | | – | mA |
| | | Digital Inputs = 0V or $V_{DD}$, $T_A$ = +25°C | | | 100 | | | – | µA |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 500 | | | – | µA |
| **SWITCHING CHARACTERISTICS** (100% tested) See Timing Diagram | | | | | | | | | |
| Chip Select To Write Setup Time | $t_{CS}$ | $T_A$ = +25°C | 200 | | | – | | | ns |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | 230 | | | – | | | ns |
| Chip Select To Write Hold Time | $t_{CH}$ | $T_A$ = +25°C | 20 | | | – | | | ns |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | 30 | | | – | | | ns |
| DAC Select To Write Setup Time | $t_{AS}$ | $T_A$ = +25°C | 200 | | | – | | | ns |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | 230 | | | – | | | ns |
| DAC Select To Write Hold Time | $t_{AH}$ | $T_A$ = +25°C | 20 | | | – | | | ns |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | 30 | | | – | | | ns |
| Write Pulse Width | $t_{WR}$ | $T_A$ = +25°C | 180 | | | – | | | ns |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | 200 | | | – | | | ns |
| Data Setup Time | $t_{DS}$ | $T_A$ = +25°C | 110 | | | – | | | ns |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | 130 | | | – | | | ns |
| Data Hold Time | $t_{DH}$ | $T_A$ = +25°C | 0 | | | – | | | ns |

NOTES: (1) Specifications apply to both DACs. (2) Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = $V_{REF}$. (3) Guaranteed, but not tested. (4) These characteristics are for design guidance only and are not subject to test.

## DICE INFORMATION
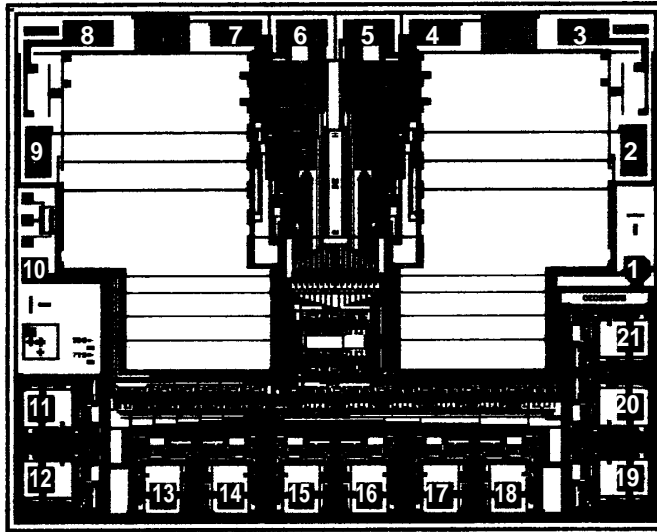


**DAC7528  TOPOGRAPHY**

| PAD | FUNCTION | PAD | FUNCTION | PAD | FUNCTION |
|-----|----------|-----|----------|-----|----------|
| 1 | $V_{DD}$ | 8 | $R_{FB\ A}$ | 15 | DB4 |
| 2 | $V_{REF\ B}$ | 9 | $V_{REF\ B}$ | 16 | DB3 |
| 3 | $R_{FB\ B}$ | 10 | DGND | 17 | DB2 |
| 4 | OUTB | 11 | $\overline{DAC\ A}$/DAC B | 18 | DB1 |
| 5 | AGNDB | 12 | DB7 | 19 | DB0 |
| 6 | AGNDA | 13 | DB6 | 20 | $\overline{CS}$ |
| 7 | OUTA | 14 | DB5 | 21 | $\overline{WR}$ |

### MECHANICAL INFORMATION

| | MILS (0.001") | MILLIMETERS |
|---|---|---|
| Die Size | 104 x 124 | 2.6 x 3.1 |
| Die Thickness | 20 ±3 | 0.51 ±0.08 |
| Min. Pad Size | 4 x 4 | 0.10 x 0.10 |

## ELECTRICAL, (DICE)

At $V_{DD}$ = +5V; $V_{REFA,\ B}$ = +10V; $I_{OUT}$ = GND = 0V: T = Full Temperature Range specification under Absolute Maximum Ratings unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | DAC7528AD | | | UNITS |
|-----------|--------|------------|-----|-----|-----|-------|
| | | | MIN | TYP | MAX | |
| **DC ACCURACY** [1] | | | | | | |
| Resolution | N | | 8 | | | Bits |
| Relative Accuracy | INL | | | | ±1 | LSB |
| Differential Nonlinearity | DNL | Guaranteed  Monolithic Over Temp | | | ±1 | LSB |
| FS Gain Error [2] | | $T_A$ = +25°C | | | ±2 | LSB |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | ±4 | LSB |
| Gain Tempco [2, 3] | | | | ±2 | ±35 | ppm/°C |
| Supply Rejection | PSR | $\Delta V_{DD}$ = ±5%, $T_A$ = +25°C | | 0.001 | 0.01 | %FSR/% |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | 0.001 | 0.01 | %FSR/% |
| Output Leakage Current (OUTA) | | DACA = $00_{16}$ $T_A$ = +25°C | | | ±50 | nA |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | ±200 | nA |
| Output Leakage Current (OUTB) | | DACB = $00_{16}$ $T_A$ = +25°C | | | ±50 | nA |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | ±200 | nA |
| **REFERENCE INPUT** | | | | | | |
| Input Resistance | | ($V_{REF\ A}$, $V_{REF\ B}$) | 8 | 10 | 15 | kΩ |
| Input Resistance Match | | ($V_{REF\ A}$, $V_{REF\ B}$) | | | ±1 | % |

NOTES: (1) Specifications apply to both DACs. (2) Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = $V_{REF}$. (3) Guaranteed, but not tested. (4) These characteristics are for design guidance only and are not subject to test.
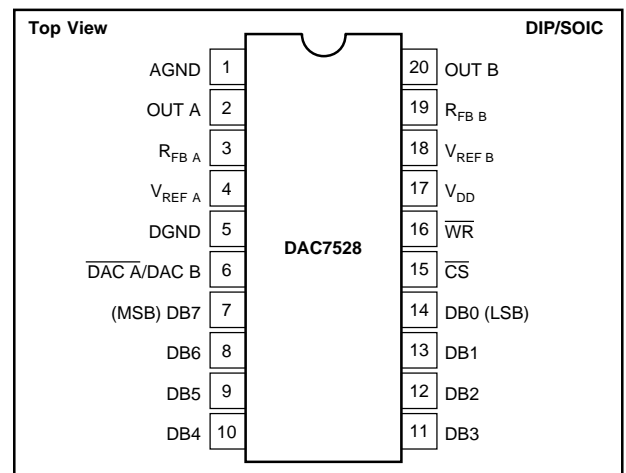
## PACKAGE INFORMATION

| MODEL | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|-------|---------|---------------------------|
| DAC7528P | 20-Pin Plastic DIP | 222 |
| DAC7528PB | 20-Pin Plastic DIP | 222 |
| DAC7528U | 20-Pin SOIC | 221 |
| DAC7528UB | 20-Pin SOIC | 221 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

## ORDERING INFORMATION

| MODEL | INL | PACKAGE | TEMPERATURE RANGE |
|-------|-----|---------|-------------------|
| DAC7528P | ±1LSB | 20-Pin Plastic DIP | −40°C to +85°C |
| DAC7528PB | ±1/2LSB | 20-Pin Plastic DIP | −40°C to +85°C |
| DAC7528U | ±1LSB | 20-Pin SOIC | −40°C to +85°C |
| DAC7528UB | ±1/2LSB | 20-Pin SOIC | −40°C to +85°C |

## PIN CONFIGURATION

**Top View**      **DIP/SOIC**

| | | DAC7528 | | |
|---|---|---|---|---|
| AGND | 1 | | 20 | OUT B |
| OUT A | 2 | | 19 | $R_{FB\ B}$ |
| $R_{FB\ A}$ | 3 | | 18 | $V_{REF\ B}$ |
| $V_{REF\ A}$ | 4 | | 17 | $V_{DD}$ |
| DGND | 5 | | 16 | $\overline{WR}$ |
| $\overline{DAC\ A}$/DAC B | 6 | | 15 | $\overline{CS}$ |
| (MSB) DB7 | 7 | | 14 | DB0 (LSB) |
| DB6 | 8 | | 13 | DB1 |
| DB5 | 9 | | 12 | DB2 |
| DB4 | 10 | | 11 | DB3 |

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## ABSOLUTE MAXIMUM RATINGS

V$_{DD}$ to GND ..................................................................... 0V, +7V
V$_{REFA, B}$ to GND ............................................................... ±25V
R$_{FA,B}$ to GND ................................................................... ±25V
Digital Input Voltage Range ................................. −0.3V to V$_{DD}$
Output Voltage (pins 2, 20) .................................. −0.3V to V$_{DD}$
Operating Temperature Range U,P .................−40°C to +85°C
　　　　　　　　　　　　　DICE .............................. 0°C to +70°C
Junction Temperature ........................................................ +150°C
Storage Temperature .....................................−60°C to +150°C
Lead Temperature (soldering, 10s) ........................................ +300°C
θ$_{JA}$　U package ............................................................ 105°C/W
　　　P package ............................................................... 85°C/W
θ$_{JC}$　U package .............................................................. 60°C/W
　　　P package ............................................................... 35°C/W

NOTES: θ$_{JA}$ is specified for worst case mounting conditions, i.e., θ$_{JA}$ is specified for device in socket for PDIP package.
**CAUTION: (1) Do not apply voltages higher than V$_{DD}$ or less than GND potential on any terminal except V$_{REFA, B}$ (pins 4 and 18) and R$_{FBA, B}$ (pins 3 and 19). (2) The digital control inputs are zener-protected: however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use. (3) Use proper antistatic handling procedures. (4) Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.**

## WRITE CYCLE TIMING DIAGRAM



NOTE: All input signal rise and fall times are measured from 10% to 90% of V$_{DD}$. V$_{DD}$ = +5V, t$_r$ = t$_f$ = 20ns; V$_{DD}$ = +15V, t$_r$ = t$_f$ = 40ns. Timing measurement reference level is (V$_{IH}$ + V$_{IL}$)/2.
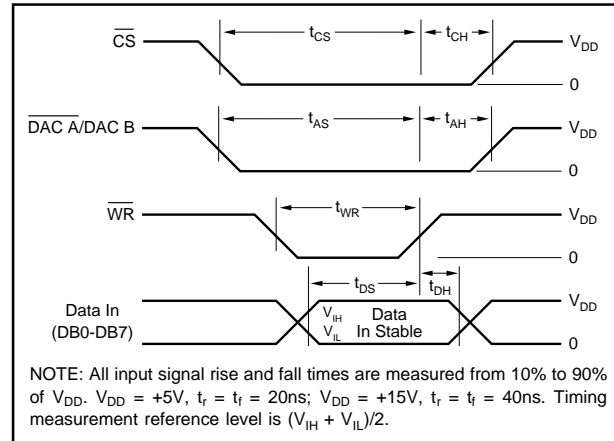
## MODE SELECTION TABLE

| DAC A/DAC B | CS | WR | DAC A | DAC B |
|---|---|---|---|---|
| L | L | L | WRITE | HOLD |
| H | L | L | HOLD | WRITE |
| X | H | X | HOLD | HOLD |
| X | X | H | HOLD | HOLD |

# ⚠ ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

*Digital Inputs:* All digital inputs of the DAC7528 incorporate on-chip ESD protection circuitry. This protection is designed and has been tested to withstand five 2500V positive and negative discharges (100pF in series with 1500Ω) applied to each digital input.

*Analog Pins:* Each analog pin has been tested to Burr-Brown's analog ESD test consisting of five 1000V positive and negative discharges (100pF in series with 1500Ω) applied to each pin. R$_{FB A}$, V$_{REF A}$, R$_{FB B}$, and V$_{REF B}$ show some sensitivity.

# TYPICAL PERFORMANCE CURVES

At V$_{DD}$ = +5V; V$_{REFA,B}$ = +10V; I$_{OUT}$ = GND = 0V: T = Full Temperature Range Specification under Absolute Maximum Ratings unless otherwise noted.



SUPPLY CURRENT vs DIGITAL INPUT VOLTAGE



DAC7528 GAIN TC
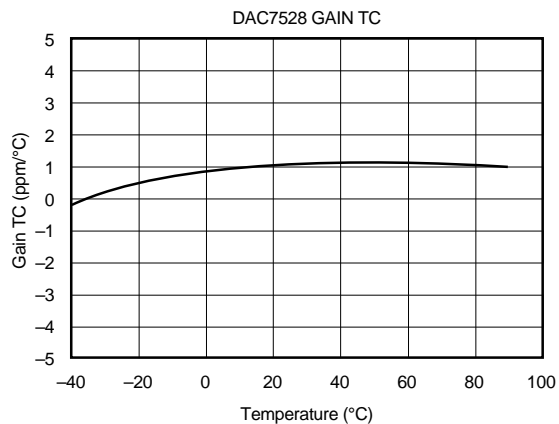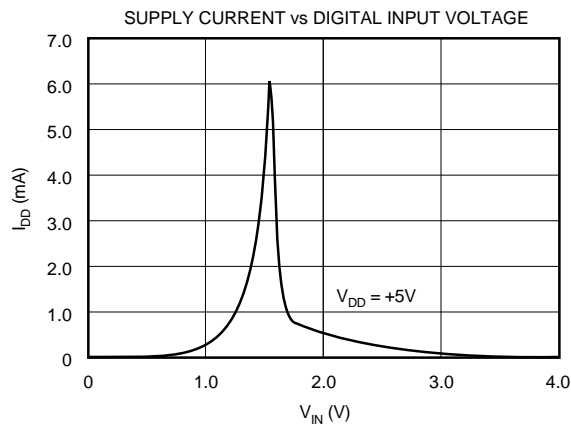
# DISCUSSION OF SPECIFICATIONS

## RELATIVE ACCURACY

This term, also known as end point linearity or integral linearity, describes the transfer function of analog output to digital input code. Relative accuracy describes the deviation from a straight line, after zero and full scale errors have been adjusted to zero.

## DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1LSB change in the output when the input code changes by 1LSB. A differential nonlinearity specification of 1LSB maximum guarantees monotonicity.

## GAIN ERROR

Gain error is the difference between the full-scale DAC output and the ideal value. The ideal full scale output value for the DAC7528 is $-(255/256)V_{REF}$. Gain error may be adjusted to zero using external trims as shown in Figure 4.

## OUTPUT LEAKAGE CURRENT

The current which appears at $I_{OUT\ A}$ and $I_{OUT\ B}$ with the DAC loaded with all zeros.

## OUTPUT CAPACITANCE

The parasitic capacitance measured from $I_{OUT\ A}$ or $I_{OUT\ B}$ to AGND.

## CHANNEL-TO-CHANNEL ISOLATION

The AC output error due to capacitive coupling from DAC A to DAC B or DAC B to DAC A.

## AC FEEDTHROUGH ERROR

The AC output error due to capacitive coupling from $V_{REF}$ to $I_{OUT}$ with the DAC loaded with all zeros.

## OUTPUT CURRENT SETTLING TIME

The time required for the output current to settle to within ±0.195% of final value for a full scale step.

## DIGITAL-TO-ANALOG IMPULSE

The integrated area of the glitch pulse measured in nanovolt-seconds. The key contributor to digital-to-analog glitch is charge injected by digital logic switching transients.

## DIGITAL CROSSTALK

Glitch impulse measured at the output of one DAC but caused by a full scale transition on the other DAC. The integrated area of the glitch pulse is measured in nanovolt-seconds.

# CIRCUIT DESCRIPTION

Figure 1 shows a simplified schematic of one half of a DAC7528. The current from the $V_{REF\ A}$ pin is switched between $I_{OUT\ A}$ and AGND by 8 single-pole double-throw CMOS switches. This maintains a constant current in each leg of the ladder regardless of the input code. The input resistance at $V_{REF\ A}$ is therefore constant and can be driven by either a voltage or current, AC or DC, positive or negative polarity, and have a voltage range up to ±20V.
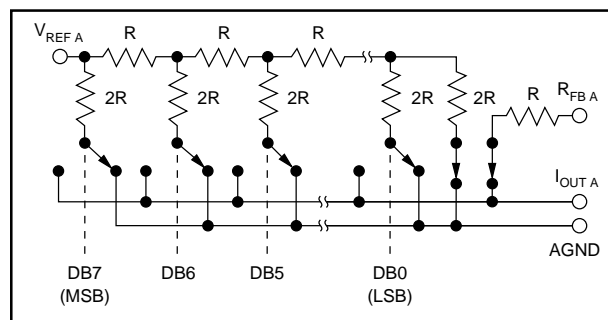


FIGURE 1. Equivalent Circuit for DAC A.

A CMOS switch transistor, included in series with the ladder terminating resistor and in series with the feedback resistor, $R_{FB\ A}$, compensates for the temperature drift of the ON resistance of the ladder switches.

Figure 2 shows an equivalent circuit for DAC A. $C_{OUT}$ is the output capacitance due to the N-channel switches and varies from about 30pF to 70pF with digital input code. The current source $I_{LKG}$ is the combination of surface and junction leakages to the substrate. $I_{LKG}$ approximately doubles every 10°C. $R_O$ is the equivalent output resistance of the D/A and it varies with input code.
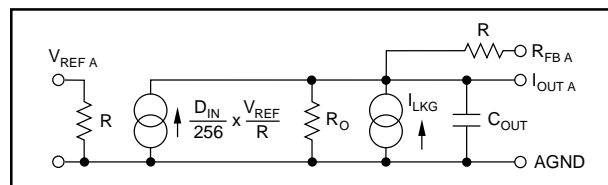


FIGURE 2. Simplified Circuit Diagram for DAC A.

# INSTALLATION

## ESD PROTECTION

All digital inputs of the DAC7528 incorporate on-chip ESD protection circuitry. This protection is designed to withstand 2.5kV (using the Human Body Model, 100pF and 1500Ω). However, industry standard ESD protection methods should be used when handling or storing these components. When not in use, devices should be stored in conductive foam or rails. The foam or rails should be discharged to the destination socket potential before devices are removed.

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## POWER SUPPLY CONNECTIONS

The DAC7528 is designed to operate on $V_{DD} = +5V \pm 10\%$. For optimum performance and noise rejection, power supply decoupling capacitors $C_D$ should be added as shown in the application circuits. These capacitors (1μF tantalum recommended) should be located close to the D/A. AGND and DGND should be connected together at one point only, preferably at the power supply ground point. Separate returns minimize current flow in low-level signal paths if properly connected. Output op amp analog common (+ input) should be connected as near to the AGND pin of the DAC7528 as possible.

## WIRING PRECAUTIONS

To minimize AC feedthrough when designing a PC board, care should be taken to minimize capacitive coupling between the $V_{REF}$ lines and the $I_{OUT}$ lines. Similarly, capacitive coupling between DACs may compromise the channel-to-channel isolation. Coupling from any of the digital control or data lines might degrade the glitch and digital crosstalk performance. Solder the DAC7528 directly into the PC board without a socket. Sockets add parasitic capacitance (which can degrade AC performance).

## AMPLIFIER OFFSET VOLTAGE

The output amplifier used with the DAC7528 should have low input offset voltage to preserve the transfer function linearity. The voltage output of the amplifier has an error component which is the offset voltage of the op amp multiplied by the "noise gain" of the circuit. This "noise gain" is equal to $(R_F/R_O + 1)$ where $R_O$ is the output impedance of the D/A $I_{OUT}$ terminal and $R_F$ is the feedback network impedance. The nonlinearity occurs due to the output impedance varying with code. If the 0 code case is excluded (where $R_O$ = infinity), the $R_O$ will vary from R to 3R providing a "noise gain" variation between 4/3 and 2. In addition, the variation of $R_O$ is nonlinear with code, and the largest steps in $R_O$ occur at major code transitions where the worst differential nonlinearity is also likely to be experienced. The nonlinearity seen at the amplifier output is $2V_{OS} - 4V_{OS}/3 = 2V_{OS}/3$. Thus, to maintain good nonlinearity the op amp offset should be much less than 1/2LSB.

## UNIPOLAR CONFIGURATION

Figure 3 shows DAC7528 in a typical unipolar (two-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table I. The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, or a dual amplifier such as the OPA2107. C1 and C2 provide phase compensation to minimize settling time and overshoot when using a high speed operational
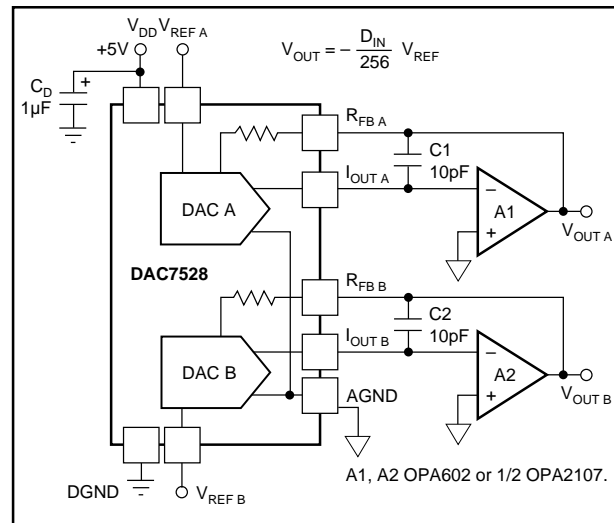


FIGURE 3. Unipolar Configuration 2 Quadrant Multiplication.

amplifier.

If an application requires the D/A to have zero gain error, the circuit shown in Figure 4 may be used. Resistors R2 and R4 induce a positive gain error greater than worst-case initial negative gain error. Trim resistors R1 and R3 provide a variable negative gain error and have sufficient trim range to correct for the worst-case initial positive gain error plus the error produced by R2 and R4.

## BIPOLAR CONFIGURATION

Figure 5 shows the DAC7528 in a typical bipolar (four-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table II.

The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, a dual amplifier such as the OPA2107, or a quad amplifier like the OPA404. C1 and C2 provide phase compensation to minimize settling time and overshoot when using a high speed operational amplifier. The bipolar offset resistors R1–R3 and R4–R6 should be ratio-matched to 0.195% to ensure the specified gain error performance.

# APPLICATION INFORMATION



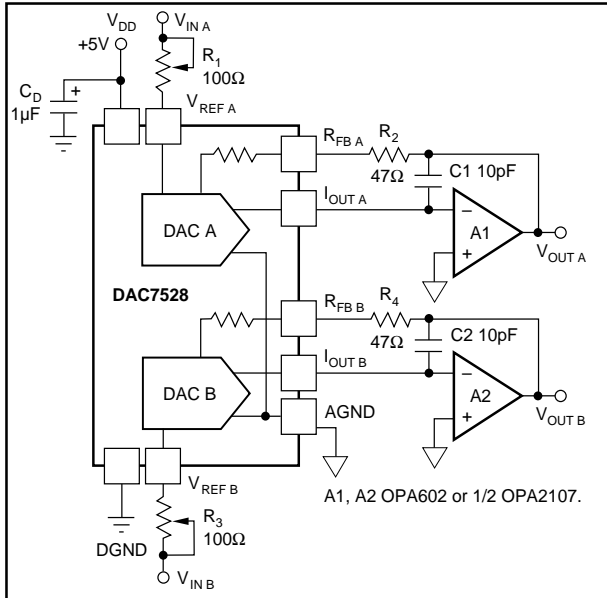FIGURE 4. Unipolar Configuration with Gain Trim.

| DATA INPUT | ANALOG OUTPUT |
|---|---|
| MSB ↓     ↓ LSB | |
| 1111 1111 | $-V_{REF}$ (255/256) |
| 1000 0000 | $-V_{REF}$ (255/256) = $-1/2 V_{REF}$ |
| 0000 0001 | $-V_{REF}$ (1/256) |
| 0000 0000 | 0V |

TABLE I. Unipolar Output Code.

| DATA INPUT | ANALOG OUTPUT |
|---|---|
| MSB ↓     ↓ LSB | |
| 1111 1111 | $+V_{REF}$ (127/128) |
| 1000 0001 | $+V_{REF}$ (1/128) |
| 1000 0000 | 0V |
| 0111 1111 | $-V_{REF}$ (1/128) |
| 0000 0000 | $-V_{REF}$ (127/128) |

TABLE II. Bipolar Output Code.
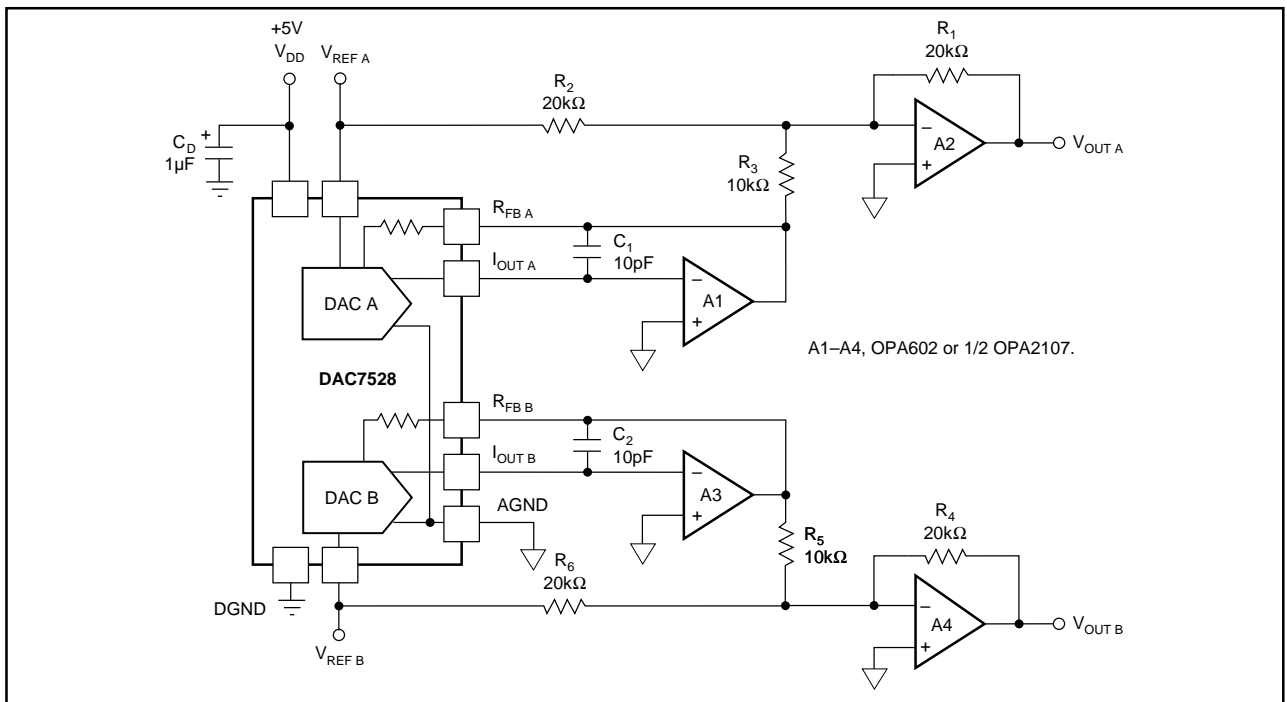


FIGURE 5. Bipolar Configuration 4 Quadrant Multiplication.

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## APPLICATIONS CIRCUIT: 8-BIT PLUS SIGN DAC



The DACs are loaded with same 8-bit word, except that one code is inverted first.
If sign bit = 1; invert DAC B's data.
If sign bit = 0; invert DAC A's data.

A1 OPA602 or 1/2 OPA2107.

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